What is Claimed is:

1. A common carrier, comprising:

a carrier substrate having an upper surface; and

a plurality of integrated chips, the integrated chips being first adhered to the upper surface of the carrier substrate in their unprocessed, integrateable chip form according to a placement alignment tolerance and then lithographically processed to form the integrated chips, wherein the integrated chips are aligned according to lithographic alignment tolerance with each other and the substrate.

2. The common carrier as described in Claim 1, wherein the unprocessed integrateable form of the integrated chips are adhered to the carrier substrate using an adhesive which retains adherence reliability when exposed to subsequent processing steps performed on the common carrier.

3. The common carrier as described in Claim 1, wherein the carrier substrate, the adhesive, and the integrated chips have essentially the same coefficient of thermal expansion (CTE).

4. The common carrier as described in Claim 1 wherein the carrier substrate comprises one of polysilicon, glass, metal, and ceramic.

5. The common carrier as described in Claim 1, wherein the carrier substrate includes a plurality of slots for adhering the plurality of chips, one chip per slot.

6. The common carrier as described in Claim 5, wherein the carrier substrate and the integrated chips each have parallel top surfaces which reside essentially within the same plane.

7. The common carrier as described in Claim 6, wherein the upper surface of the carrier substrate and the unprocessed, integrateable form of the integrated chips are polished prior to being lithographically processed.

8. The common carrier as described in Claim 1, wherein the carrier substrate and the integrated chips each have parallel top surfaces which do not reside within the same plane.

9. The common carrier as described in Claim 8, wherein the unprocessed, integrateable chip form of the plurality of chips is lithographically processed using a curtain coating photoresist deposition.

10. The common carrier as described in Claim 7 further comprising a filler material adapted to fill a peripheral gap between the interior edges of each of the slots and the peripheral edges of each of the unprocessed, integrateable form of the integrated chips when each chip is adhered within each slot and prior to being polished.

11. The common carrier as described in Claim 9 wherein the filler material comprises glass frit.

12. The common carrier as described in Claim 1 further comprising:

at least two electrically conductive nodes, the electrically conductive nodes are disposed on either one of the chip and the carrier substrate; and

an interconnect adapted to electrically connect the electrically conductive nodes.

13. The common carrier of Claim 1, wherein the plurality of integrated chips is a component selected from a group consisting of an inkjet printhead, a thermal inkjet printhead, a semiconductor, an integrated circuit, an ASIC, a MicroElectroMechanical System, and a fluidic device.

14. A method of forming a common carrier comprising the steps of:

adhering an unprocessed, integrateable form of a plurality of chips on the upper surface of a carrier substrate according to a first placement alignment precision;

lithographically processing the unprocessed, integrateable form of the plurality of chips to form a plurality of integrated chips on the upper surface, wherein the integrated chips are aligned with each other and the substrate with a second alignment precision having lithographic processing tolerances.

15. The method of forming the common carrier as described in Claim 14 wherein the first alignment precision has a greater tolerance range than the lithographic processing tolerances.

16. The method of forming the common carrier as described in Claim 14 wherein the first alignment precision has a tolerance in the range of +/- 1 milimeter and the second alignment precision has a tolerance in the range of less than 1 micron.

17. The method of forming the common carrier as described in Claim 14 further comprising the steps of:

forming a plurality of slots within the upper surface of the carrier substrate according to the first alignment precision; and

adhering the unprocessed, integrateable form of the integrated chips within the plurality of slots.

18. The method of forming the common carrier as described in Claims 17 further comprising the step of depositing a filler so as to fill a peripheral gap between the interior edges of each of the slots and the peripheral edges of each of the unprocessed, integrateable form of the integrated chips when each unprocessed chip is adhered within each slot.

19. The method of forming the common carrier as described in Claim 18 further comprising the step of polishing the upper surface of the plurality of chips to be in essentially the same parallel plane as the upper surface of the carrier substrate.

20. The method of forming the common carrier as described in Claim 14 further comprising the step of adhering the unprocessed, integrateable form of the integrated chips directly on the upper surface of the carrier substrate such that the upper surface of the unprocessed, integrateable chips is in a parallel, but different, plane than the upper surface of the substrate carrier.

21. The method of forming the common carrier as described in Claim 20 further comprising the step of lithographically processing using curtain coating deposition.